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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,813	08/28/2003	Young-Hee Song	9903-078	9556

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MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,813	SONG ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2005*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,8-11,24-30,33,34,36-38,40,42 and 47-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,8-11,24-30,33,34,36-38,40,42 and 47-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/651813 Attorney's Docket #: 9903-078
Filing Date: 8/28/2003; claimed foreign priority to 7/10/2001 and 1/18/2002

Applicant: Song et al.

Examiner: Alexander Williams

This action time is restarted to the mailing of this action because claims 48-51 was not addressed in the action dated 1/27/05.

Applicant's Amendment filed 7/29/05 has been acknowledged.

Applicant's had election of the species of figure 18 (claims 1, 3, 4, 6-11, 24-30, 33, 34,36-38, 40, 42, 46, 47 and 48-51), filed 5/3/2004, has been acknowledged.

Claims 2, 5, 12-23, 31, 32, 35, 39, 41, 43-46 have been cancelled.

Again, acknowledgment is made of applicant's claim for foreign priority based on an application filed in Republic of Korea on 7/10/2001 and 1/18/2002. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b).

The disclosure is objected to because of the following informalities: Applicant's related application information should be updated.

Appropriate correction is required.

Claims 36 to 38, 40 and 42 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 36 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language. This claim is an omnibus type claim. In this independent claim, it claims "a second bond pad-wiring pattern"; a second pad-rearrangement pattern"; and "a second insulating layer" without previously claiming "a first bond pad-wiring pattern"; "a first pad-rearrangement pattern"; and a first insulating layer."

Any of claims 36 to 38, 40 and 42 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a pad-rearrangement pattern(s) and a wiring layer and solder deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1, 3, 4, 6, 8-11, 24-30, 33, 34,36-38, 40, 42, 47 and 48-53 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pai et al. (U.S. Patent # 6,503,776 B2) in view of Akram et al. (U.S. Patent # 6,228,687 B1).

1 . Pai et al. (figures 110) specifically figure 8 show a semiconductor multi-chip package comprising: a package substrate **120** including a surface having a plurality of bonding tips **120a** formed thereon; and two or more semiconductor chips **110,130** mounted on the substrate surface. Pai et al. fail to explicitly show the two or more semiconductor

chips each including: a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other; a bond pad-wiring pattern formed on the semiconductor substrate; and a pad-rearrangement pattern directly contacting the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region, wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate, wherein each bonding tip is electrically connected to a corresponding one of the bond pads, wherein each bonding tip is electrically connected to a corresponding one of the bond pads.

Akram et al. is cited for showing a wafer-level package. Specifically, Akram et al. (figures 1 to 10) specifically figures 8A and 8B discloses semiconductor chip **210** each including: a semiconductor substrate **212** having integrated circuits formed on a cell region (within 212) and a peripheral circuit region adjacent to each other; a bond pad-wiring pattern **216** formed on the semiconductor substrate; and a pad-rearrangement pattern **222,228** directly contacting the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads **221** disposed over at least a part of the cell region, wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate for the purpose of forming a desired semiconductor integrated circuit in the internal circuit region for a semiconductor integrated circuit device.

(22) FIGS. 8A and 8B illustrate another embodiment of a chip-scale package 210, which includes a semiconductor device 212 and a carrier substrate 218 disposed adjacent an active surface 214 of semiconductor device 212.

(23) As illustrated, semiconductor device 212 is a leads over chip ("LOC") type semiconductor device, which includes bond pads 216 disposed substantially linearly across the center of semiconductor device 212. A conductive bump 217 may be disposed on each bond pad 216 or on a BLM or UBM structure adjacent to each bond pad 216.

(24) Carrier substrate 218 comprises an insulative layer 220, preferably formed of polymeric material, such as polyimide or another non-conductive elastomer, and has a substantially consistent thickness. Bond pads 216 of semiconductor device 212 or conductive bumps 217 are exposed through layer 220 through one or more apertures 228. An adhesive film layer 230 is disposed adjacent layer 220, opposite semiconductor device 212. Adhesive film layer 230 carries conductive traces 222 and

external package bumps 224. External package bumps 224 protrude from adhesive film layer 230. Conductive traces 222 are in electrical communication with corresponding external package bumps 224 and extend across adhesive film layer 230 to corresponding vias 221. Vias 221, which communicate with conductive traces 222, extend through adhesive film layer 230, into apertures 228, and into electrical communication with corresponding bond pads 216.

(25) As illustrated in FIGS. 8A and 8B, each conductive trace 222 communicates with a corresponding external package bump 224. Thus, each bond pad 216 that communicates with a conductive trace 222 may also communicate with a laterally offset, corresponding external package bump 224. Alternatively, as illustrated in FIG. 8C, each conductive trace 222 may communicate with a group or an array of external package bumps 224'.

(26) FIG. 8D illustrates a variation of chip-scale package 210', which includes a semiconductor device 212' having peripherally located bond pads 216' and external package bumps 224' disposed in an array on adhesive film layer 230'.

3. The multi-chip package of claim 1, the combination with Pai et al. showing wherein the two or more chips are vertically stacked.

4. The multi-chip package of claim 1, the combination with Pai et al. showing wherein the two or more chips comprise the same type of chips.

6. The multi-chip package of claim 1, the combination with Pia et al. wherein one of the two or more chips is a memory chip and the other chip is a non-memory chip (see column 1, lines 5-32).

8. The multi-chip package of claim 1, the combination with Akram et al. showing wherein the bond pads are formed along sides of the semiconductor substrate.

9. The multi-chip package of claim 1, the combination with Akram et al. showing wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

10. The multi-chip package of claim 1, the combination with Akram et al. showing wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

11. The multi-chip package of claim 1, the combination with Akram et al. showing wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

24. Pai et al. (figures 110) specifically figure 8 show a multi-chip package comprising: a first chip **110**; and a second chip **130** formed over the first chip. Pai et al. fail to explicitly show the first chip includes: a bond pad-wiring pattern formed substantially in a center region of the first chip; and a pad-rearrangement pattern directly contacting the bond pad-wiring pattern; and an insulating layer formed on the pad-rearrangement pattern, wherein the pad-rearrangement pattern includes a first bond pad disposed at an edge of the first chip, wherein the first bond pad is exposed through the insulating layer.

Akram et al. is cited for showing a wafer-level package. Specifically, Akram et al. (figures 1 to 10) specifically figures 8A and 8B discloses semiconductor chip **210** each including: a semiconductor substrate **212** having integrated circuits formed on a cell region (within 212) and a peripheral circuit region adjacent to each other; a bond pad-wiring pattern **216** formed on the semiconductor substrate; and a pad-rearrangement pattern **222,228** directly contacting the bond pad-wiring pattern; and an insulating layer **220** formed on the pad-rearrangement pattern, wherein the first bond pad is exposed through the insulating layer, the pad-rearrangement pattern including bond pads **221** disposed over at least a part of the cell region, wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate for the purpose of forming a desired semiconductor integrated circuit in the internal circuit region for a semiconductor integrated circuit device.

25. The multi-chip package of claim 24, the combination with Akram et al. showing wherein the pad-rearrangement pattern includes a second bond pad, and wherein the first and second bond pads are respectively disposed along opposing edges of the first chip.

26. The multi-chip package of claim 25, the combination with Akram et al. showing wherein the pad-rearrangement pattern extends substantially from the center region of the first chip toward the edge of the first chip.

27. The multi-chip package of claim 24, the combination with Akram et al. showing wherein the bond pad-wiring pattern is formed on a first surface of the first chip, and Pai et al. show wherein the second chip is mounted on the first surface of the first chip.

28. The multi-chip package of claim 27, the combination with Pai et al. showing further comprising a spacer **160** interposed between the first chip and the second chip.
29. The multi-chip package of claim 24, the combination with Pai et al. showing further comprising a substrate **120** on which the first chip is mounted.
30. The multi-chip package of claim 29, the combination with Pai et al. showing wherein the substrate **120** comprises a printed circuit board, a tape wiring substrate or a lead frame.
33. The multi-chip package of claim 24, the combination show wherein the first bond pad is disposed under the second chip. It is unclear what is claimed here.
34. The multi-chip package of claim 24, the combination with Pai et al. showing wherein the first **110** and second **130** chips comprise the same type of chips.
36 and similiar claim 53. Pai et al. (figures 110) specifically figure 8 show a multi-chip package comprising: a first chip **110**; and a second chip **130** formed over the first chip **110**. Pai et al. fail to explicitly show wherein the second chip includes: a second bond pad-wiring pattern formed substantially in a center region of the second chip; and a second pad-rearrangement pattern electrically connected to the second bond pad-wiring pattern, wherein the second pad-rearrangement pattern includes a second bond pad disposed at an edge of the second chip.

Akram et al. is cited for showing a wafer-level package. Specifically, Akram et al. (figures 1 to 10) specifically figures 8A and 8B discloses semiconductor chip **210** each including: a semiconductor substrate **212** having integrated circuits formed on a cell region (within 212) and a peripheral circuit region adjacent to each other; a bond pad-wiring pattern **216** formed on the semiconductor substrate; and a pad-rearrangement pattern **222,228** directly contacting the bond pad-wiring pattern; and a second insulating layer **220** formed on the second pad-arrangement pattern, wherein the second bond pad is exposed through the second insulating layer, the pad-rearrangement pattern including bond pads **221** disposed over at least a part of the cell region, wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate for the purpose of forming a desired semiconductor integrated circuit in the internal circuit region for a semiconductor integrated circuit device.
37. The multi-chip package of claim 36, the combination with Pia et al. showing wherein the first chip includes; a first bond pad-wiring pattern formed substantially in a center region of the first chip; and a first pad-rearrangement pattern electrically connected to

the first bond pad-wiring pattern, wherein the first pad-rearrangement pattern includes a first bond pad disposed at an edge of the first chip.
38. The multi-chip package of claim 37, the combination with Akram et al. showing wherein the first bond pad-wiring pattern is formed on a first surface of the first chip, and wherein the second chip is mounted on the first surface of the first chip.
40. The multi-chip package of claim 36, Pai et al. further comprising a substrate **120** on which the first chip is mounted.
42. The multi-chip package of claim 40, the combination with Akram et al. showing wherein the first chip includes a center pad-type bond pad.
46. (but now claim 47). Pai et al. (figures 110) specifically figure 8 show a semiconductor multi-chip package comprising: a first chip **110** mounted on a package substrate; and an second chip **130** mounted on the first chip with a spacer **160** disposed therebetween, wherein the spacer is placed between the bond pads.
48. The semiconductor multi-chip package of claim 47, the combination with Pia et al. showing wherein the spacer is disposed over the bond pad-wiring patterns formed substantially in a center region of the first chip.
49. The semiconductor multi-chip package of claim 48, the combination with Pia et al. showing wherein each bonding tip is electrically connected to a corresponding one of the bond pads through a bonding wire.
50. The semiconductor multi-chip package of claim 49, the combination with Pia et al. showing wherein the two or more chips comprise at least a lower chip and an upper chip, the upper chip disposed over the lower chip, and wherein the spacer provides a sufficient space between the lower chip and the upper chip for the bonding wire to connect the lower chip with the package substrate.
51. The semiconductor multi-chip package of claim 1, the combination with Akram et al. showing wherein the cell region comprises a memory cell array region.

Pai et al. fail to explicitly show wherein the first chip includes; bond pad-wiring patterns formed substantially in a center region of the first chip; and pad-rearrangement patterns electrically connected to the bond pad-wiring patterns, wherein the pad-rearrangement patterns include bond pads disposed along opposing edges of the first chip.

Akram et al. is cited for showing a wafer-level package. Specifically, Akram et al. (figures 1 to 10) specifically figures 8A and 8B discloses semiconductor chip **210** each

including: a semiconductor substrate **212** having integrated circuits formed on a cell region (within 212) and a peripheral circuit region adjacent to each other; a bond pad-wiring pattern **216** formed on the semiconductor substrate; and a pad-rearrangement pattern **222,228** directly contacting the bond pad-wiring pattern; and insulating layers **220** formed on the pad-rearrangement patterns, the pad-rearrangement pattern including bond pads **221** disposed over at least a part of the cell region, wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate for the purpose of forming a desired semiconductor integrated circuit in the internal circuit region for a semiconductor integrated circuit device.

Therefore, it would have been obvious to one of ordinary skill in the art to use Akram et al.'s internal structure of a chip to modify Pai et al.'s chip for the purpose of forming a desired semiconductor integrated circuit in the internal circuit region for a semiconductor integrated circuit device.

Therefore, it would have been obvious to one of ordinary skill in the art to use the pad arrangement pattern or patterns and the wiring layer and solder bump as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Pai et al. (U.S. Patent # 6,503,776 B2) in view of Akram et al. (U.S. Patent # 6,228,687 B1) and further in view of Hsuan et al. (U.S. Patent # 6,239,366 B1).

The combination of Akram et al. and Pai et al. show the features of the claimed invention as detailed, but fail to explicitly show one of the two or more chips is a DRAM and the other chip is a flash memory.

Hsuan et al. Is cited for showing a face to face multi-chip package. Specifically, Hsuan et al. (figures 3A to 5D) specifically figure 3a discloses stacked dies, wherein one of the two or more chips is a DRAM and the other chip is a flash memory for the purpose of providing multi-chip packages to enhance the performance of the chips.

In a multi-chip package, chips of processor, memory, including dynamic random access memory (DRAM) and flash memory, and logic circuit can be packed together in a single package to reduce the fabrication cost and the packaging volume. Furthermore, the signal transmission path is shortened to enhance the efficiency.

Therefore, it would have been obvious to one of ordinary skill in the art to use Huang et al.'s a DRAM and the other chip is a flash memory and Akram et al.'s internal structure of a chip to modify Pai et al.'s chip for the purpose of forming a desired semiconductor integrated circuit in the internal circuit region for a semiconductor integrated circuit device.

Response

Applicant's arguments filed 7/29/05 have been fully considered, but are moot in view of the modified grounds of rejections detailed above. Applicant's arguments have been fully considered but are not found to be persuasive in view of the revised rejections detailed above. Applicant's claims "a pad-rearrangement pattern(s) directly contacting the bonding pad-wiring pattern(s)" in most of the independent claims above. This language can still be met by The Akram reference by letting the wiring conductive layer(s) 222 and the solder ball(s) representing the pad-rearrangement pattern. Akram's insulating layer 220 represents the claimed "insulating layer(s) formed on the pad-rearrangement patterns."

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,734,777,784,786,728,724,725,698,690,203, 211,208	6/24/04 1/22/05 10/3/05
Other Documentation: foreign patents and literature in 257/686,685,734,777,784,786,728,724,725,698,690,203, 211,208	6/24/04 1/22/05 10/3/05
Electronic data base(s): U.S. Patents EAST	6/24/04 1/22/05 10/3/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
10/5/05

Primary Patent Examiner
Alexander O. Williams